

### **MODEL 7945**

#### **KEY FEATURES**

- Double side inspection (post-diced wafer)
- Full color defect detection
- Selectable resolution and algorithms:
  VCSELs, PDs, LEDs, and Discrete Devices
- Fast Multi-CPU image processing
- Shared auto wafer loader
- Maximum 8" wafer (10" hoop ring)

## IN-PROCESS WAFER DIE INSPECTION SYSTEM MODEL 7945

Chroma 7945 wafer chip inspection system is an automated inspection system for Pre and Post diced patterned wafers. Change kits enable switching between various applications by allowing different carriers including metal frame or grip ring.

#### **Double Side Inspection**

For compound semiconductor wafers, critical backside defects can occur during the dicing process (peeling, chipping, etc.) leading to catastrophic failure. To view such defects in traditional inspection systems the wafer (on tape) is flipped for back side inspection. This flipping with a second inspection run reduces a standard system's throughput by half, renders die loss (falling off of the inverted tape) and alignment challenges in front to backside wafer map correlation. The doublesided solution alleviates these issues as dual cameras capture the top and bottom sides simultaneously in one scan. This targeted solution yields loss free and precise wafer map correlation in one single pass.

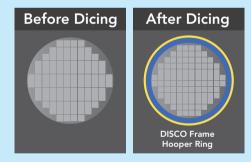
#### Color System

Discoloration can show angstrom level defects that are undetected on UV Line Scan or BW camera systems. Chroma's design identifies minimal discoloring to ensure there is not a higher overkill or underkill during the inspection process. The intuitive software assists the development of the inspection items in defined die zones according to the characteristics of color.

#### Wafer Map Format

Chroma 7945 supports traditional wafer map formats and is compatible with; .csv, SEMI XML, SNIF, STIF, and KLARF. Chroma's Mapping Software allows wafer map stacking of pre and post dicing inspection (front + back sides) as well as test yield maps to validate the dicing process and consolidate the material inspection and test yield all on one map.

#### APPLICABLE WAFER PROCESS





# Chroma

#### **APPLICATIONS**

#### Photo Diode Defect Blemish Branch Broken Pad Damage Scratch Pad Scratch Double Chip Backside Peeling Chipping VCSEL Defect **Emitter Defect** Epi Defect Emitter Discolor Pad Scratch **Outside Emitter** Backside Chipping Discolor Chipping **LED Defect**

Finger Broken

**Finger Scratch** 

Chipping

**Epitaxy Defect** Pad Lock

Epitaxy Defect

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information in Chroma ATE APP

Pad Scratch

#### **SPECIFICATIONS**

Peeling

Model	7945
Suitable Chip and Package T	
Wafer Size	≤ 8 inch (10 inch hoop ring)
Chip Size	75um x 75um ~ 8mm x 8mm
Applications	Compound semiconductors and diodes:
	VCSEL, EEL, PD, LED, FET, MOSFET
Inspection	
Camera	25M color camera x 2 (front side and back side inspection)
Light Source	LED co-axis light, ring light, back light
Magnification	2X, 5X and 10X objective lens (optional)
Resolution	1.28um/pixel (2X) ; 0.5um/pixel (5X) ; 0.25um/pixel (10X)
System	
Cassette Load Port	x 2
Warpage Compensation	Software auto focus and mechanical fix focus column to
	overcome wafer warpage
Computer	x 2 (standard), supports up to 4 image proccessors
Software Function	
Imaga Cambining	Ability to separate one larger chip into several FOV images
Image Combining	then perform inspection
Monitor	Real-time wafer map display
Image Storage	Ability to save all images or defect images
Report	Chip position, defect type, inspection analysis
Cassette Selection	Programmable selection and scheduling
Facility Requirement *1	
Dimension (W $x D x H$ )	1900 mm x 1600 mm x 2000 mm
Weight	3000 kg
Clean Room Class	Class 1000
Power	AC 220V±10%, 50/60 Hz, 1 Φ , 4.4KW
Compressed Air	0.6 MPa
Operation Temperature	+5°C ~40°C
Operation Humidity	20%~60% R.H.
Note *1: Configuration is one	loader with one inspector

\* All specifications are subject to change without notice.

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iOS

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Search Keyword

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